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(54) MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE

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CLAIMS

A manufacturing method for a semiconductor device, characterized in that a semiconductor device on the surface of which an insulating layer is provided is formed on a

semiconductor substrate, two semiconductor substrates are prepared that are obtained by forming a metallic bump that passes through a portion of the above-mentioned insulating layer, said metal bump is sufficiently coated on the surface of one or both of the semiconductor circuit substrates, moreover, a thin insulating resin adhesive layer is spin distributed wherein the surface becomes almost flat, immediately after that, said insulating resin adhesive layer is uniformly etched until the surface of the above-mentioned metallic bump appears; next, in a condition in which the front and back of these two semiconductor circuit substrates are facing mutually opposite, the metallic bumps on top of both of the semiconductor circuit substrates are made so as to mutually align and both semiconductor circuit substrates are made to contact, and by means of heating and drying said insulating resin adhesive layers, both semiconductor circuit substrates are made to adhere, and moreover, said metallic bumps are made so as to electrically contact each other.

DETAILED EXPLANATION OF THE INVENTION

INDUSTRIAL FIELD OF THE APPLICATION

This invention relates to a semiconductor integrated circuit, and specifically, it relates to a manufacturing method for a multilayer semiconductor integrated circuit that is obtained by laminating semiconductor integrated circuit substrates in which the functions are different.

PROBLEMS TO BE SOLVED BY THE INVENTION

A multilayer semiconductor integrated circuit has a construction wherein an active layer in which functional elements such as transistors, diodes, resistors, capacitors, and a metallic wiring layer that connects these functional elements are deposited on a flat surface and laminated in multilayers, and compared to the two-dimensional semiconductor integrated circuit currently known that is made up of a single functional layer, an improvement in the integration density of the integrated circuit and diversification can be expected. As a method that is currently known as a manufacturing method for a multilayer semiconductor integrated circuit, there is a multilayering method wherein: (1), on top of an insulating layer that is formed on top of a first active layer, annealing is conducted by using a laser beam, an electron beam, or a strip heater, and a recrystallized polysilicon layer (a SOI film) is formed; (2), a second layer is formed on top of this polysilicon layer, and after that, the processes are repeated (S. Kawamura, IEDM Technical Digests, p. 364, 1983). However, in this method, in order to successively form active layers, there are the shortcomings such as the fact that the manufacturing cycle becomes long, and the decrease in the yield is severe. Also, there are many new technologies that need to be

newly developed, such as the technology that smooths the surface of the each active layer, a low temperature process that manufactures active layers which are newly laminated without deteriorating the element characteristics of the lower active layers that are already formed, and technology that forms the SOI structure on a wide surface area.

PURPOSE OF THE INVENTION

The purpose of this invention is to offer a manufacturing method for a multilayer semiconductor integrated circuit that can eliminate the drawbacks of the manufacturing method for a multilayer semiconductor integrated circuit used in the past.

CONSTRUCTION OF THE INVENTION

According to this invention, a manufacturing method for a semiconductor device is obtained that is characterized in that a semiconductor device on the surface of which an insulating layer is provided is formed on a semiconductor substrate, two semiconductor substrates that are obtained by forming a metallic bump that passes through a portion of the above-mentioned insulating layer are prepared, and the metal bump is sufficiently coated on the surface of one or both of the semiconductor circuit substrates; moreover, a thin insulating resin adhesive layer is spin-distributed wherein the surface becomes almost flat, and immediately after that the insulating resin adhesive layer is uniformly etched until the surface of the above-mentioned metallic bump appears; next, in a condition in which the front and back of these two semiconductor circuit substrates are facing mutually opposite, the metallic bumps on top of both of the semiconductor circuit substrates are made so as to mutually align and both semiconductor circuit substrates are made to contact, and by means of heating and drying the insulating resin adhesive layers, both semiconductor circuit substrates are made to adhere, and moreover, the metallic bumps are made so as to electrically contact each other.

APPLICATION EXAMPLES

Below, application examples of this invention are explained in detail by using the figures. Figures 1(a) to (f) show the flow of the manufacturing method for a multilayer semiconductor integrated circuit using this invention. Figure 1(a) shows a semiconductor circuit substrate (1) on which an active layer (102), comprising active elements and metallic wiring such as aluminum that mutually connects them formed on top of a substrate (101) made of a semiconductor such as silicon or potassium and an insulating material such as silicon dioxide or sapphire, and an

insulating layer (103) of silicon dioxide or the like that protects (102), are formed. This semiconductor circuit substrate (1) is made by means of a process that manufactures the ordinary two-dimensional integrated circuit, such as, for example, the NMOS process, the PMOS process, the CMOS process, or the bipolar process.

Next, as is shown in Figure 1(b), window sections are provided in one portion of (103) on top of 1, and a metallic bump (104) of gold or the like is formed in this window section. As a means of forming [the device of] Figure 1(b), there is the method wherein, using as a mask a photoresist that is patterned by using the lithography method, after opening (103) of silicon dioxide or the like by using a chemical such as fluoric acid or the like, the film thickness of (103) is made thin by means of a high vacuum vapor deposit or the like, a metallic film of gold or the like is formed, and lastly, the photoresist is removed (called the lift-off method), and the metallic bump (104) is formed. Now then, (104) and the active layer (102) are mechanically connected.

After this, as is shown in Figure 1(c), (104) is completely coated on top of the insulating layer (103) and (104) [sic; (102)], moreover, an insulating resin adhesive of a thin film of a polyimide group resin or the like is spin coated that almost smooths the surface. For example, the height of the metallic bump is made $1.5\text{ }\mu\text{m}$ measured from the surface of the active layer (102), the thickness of the polyimide group resin is made so as to be about $2.5\text{ }\mu\text{m}$, and if the spin speed and the spin time are selected, the surface after the distribution becomes almost flat. Next, the insulating resin adhesive layer is processed in an etching plasma until the surface of the metallic bump (104) appears uniformly from the surface.

As a result of this, as is shown in Figure 1(d), a semiconductor circuit device (1) is obtained wherein the metallic bump (104) is exposed, and portions other than that are covered by a flat insulating resin adhesive layer (105). Two semiconductor circuit devices are prepared through the above process; one of the surfaces is placed facing up and the other surface is placed facing down, and alignment is conducted so that the positions of the metallic bumps that are provided on these semiconductor circuit devices mutually align (Figure 1(e)). In the above explanation, the lower semiconductor circuit device is called the first circuit device (150), and the upper semiconductor circuit device the second circuit device (151). As for the keys in the figure, (150) is used in Figure 1(d) and (151) is used for the items with the apostrophe added to the keys of Figure 1(d).

As one example of an alignment method, there is the off-axis method that uses a reduced projection exposure device. Alignment locations are provided in two locations within the aligning device. At the respective alignment locations, a stage that fastens the chip or the wafer and a matching reference mark are provided. The range of the alignment reference marks for two locations are determined beforehand. First, after (150, 151) are respectively fastened to the stage, the stage is moved, and the respective alignment marks are aligned. Next, one of them, for

example, the stage on which (150) is fastened, is moved exactly the distance between the alignment reference marks, and (150) is placed so as to come directly beneath (151). As a result of this, (150) and (151) are aligned within the mechanical precision in which the stages can be moved.

Finally, in a condition in which the relative positions in the planar direction of (150) and (151) is maintained, (105) and (105') are bonded by bringing (150) and (151) into contact, then heating; (105) and (105') are caused to adhere after drying, so that the multilayer semiconductor integrated circuit shown in Figure 1(f) can be realized. At this time, the metallic bumps (104, 104') are also fused, and (150) and (151) are electrically connected through the medium of (104, 104'). In the event (105, 105') are polyimide resins, the heating temperature is 250 to 400°C, and the time is 20 to 60 min. If a constant pressure is applied between (150) and (151') during heating, (104) and (104') are mutually fused and bonded, and besides the electrical resistance between (104, 104') becoming extremely small, the adhesive strength of (150) and (151') is also strengthened.

Figure 2 is one example of a two-layer semiconductor integrated circuit that was manufactured by using the manufacturing method of this invention. (201) is a substrate of silicon or the like for the first circuit substrate (250) (hereinafter, called the bottom layer), (202) is an insulating film of silicon dioxide or the like, (220) is a thin-film transistor for the bottom layer that is manufactured wherein the source and drain (203, 205), the channel (204), and the gate (206) are made on top of an SOI construction. (207) is the bottom layer metallic wiring, and (208) is the insulating layer for the bottom layer. Also, (209) is a metallic bump for the bottom layer, and (210) is an insulating resin adhesive layer for the bottom layer. Now then, in the second circuit substrate (251) (hereinafter, called the top layer), the elements that are the same as in the bottom layer have an apostrophe attached to the element key for the bottom layer. As is shown in Figure 2, the source and drain (205, 205') for the thin film transistors (220, 220') of the top and bottom layer are connected through the medium of the metallic-wiring (207, 207') and the metallic bump (209, 209'), and the intended circuit can be formed.

Figure 2 is shown in regard to a two-layer semiconductor integrated circuit, but if k layers and k' layers of semiconductor integrated circuits are used that are formed by using the prior methods on the top and bottom layers, respectively, a multilayer integrated circuit of $(k + k')$ layers can be realized. Or, in Figure 2, direct wiring that passes through the insulating layer (202') of the upper layer can be provided beforehand, and after laminating the top and bottom layers by using this invention, the substrate (201') is removed, and if a process is repeated that laminates a third circuit substrate by again using this invention, a multilayer semiconductor integrated circuit of three or more layers can also be realized. One example in the case of three layers being laminated is shown in Figure 3. (301) is the first circuit substrate, and is equivalent

to (250) of Figure 2. (302) is a second circuit substrate, and is equivalent to the substrate (251) of Figure 2 from which the substrate (201') has been removed. Each element in the construction of (301, 302) is equivalent to those of Figure 2. The newly added component is the gold that passes through the insulating film (202') and the [illegible] wiring (304) that is made up of aluminum or the like. (303) is the third circuit substrate. (311) is the substrate, (305) an insulating film, (306) a thin film transistor, (307) is metallic wiring, (308) an insulating film, (309) a metallic bump, and (310) is an insulating resin adhesive layer that is formed on top of the third circuit substrate. Because (306) is electrically connected to (207') through the medium of (307, 309, 209'), the first, second, and third circuit substrates are mechanically connected.

In the explanation of Figure 1, an explanation was given in regard to a case wherein an insulating resin adhesive layer was formed on a first and second circuit substrate, but it does not matter even if it is a case wherein it is formed on only one circuit substrate. Also, in Figure 2 and Figure 3, an SOI construction is shown as the circuit substrate for each layer, but it is not limited to this. It does not matter if it is completely different substrates, for example, a silicon substrate and an SOS substrate, or a silicon substrate and a potassium arsenic substrate. Or, it can be completely different functions, for example, a combination of a CMOS information circuit and an image sensor, or an information circuit used for signal processing and a photo emitter and photoreceptor element. Also, it does not matter if the size of the first circuit substrate and the second circuit substrate are different. For example, a case of laminating a plurality of small chips on a wafer scale integrated circuit can be considered.

EFFECTS OF THE INVENTION

According to this invention, because the active layers for each layer can be manufactured concurrently, the manufacturing time can be shortened compared to the manufacturing method for a multilayer semiconductor integrated circuit used in the past. Also, if the active layer for each layer is inspected beforehand, and only those that are properly made are laminated, an increase in the yield can be anticipated. Also, because a multilayer semiconductor integrated circuit can be realized by using a bulk substrate and an SOS and substrate without having the relationship of large surface area SOI [illegible] technology by means of laser annealing technology and the like, the development speed is fast. Also, the laminating process is a low temperature process, the circuit substrate surface for each layer is smoothed by a process that forms an insulating resin adhesive layer, and the like, and the drawbacks of the manufacturing methods used until now can be eliminated. Furthermore, because there are no limits to the construction and manufacturing processes for the circuit substrates of each layer, diversification

and the like and applications which could not be considered with the manufacturing method used until now also become possible.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1(a) to (f) are cross-sectional views for the purpose of explaining the flow of the manufacturing method for a multilayer semiconductor integrated circuit according to this invention. (101, 102, 103, 104, 105) are a substrate, an active layer, an insulating layer, a metallic bump, and an insulating resin adhesive layer, respectively. Also, (150, 151) are the first circuit substrate and the second circuit substrate. Figure 2 and Figure 3 are cross-sectional views of application examples of this invention, and are diagrams showing a two-layer semiconductor integrated circuit and a three-layer semiconductor integrated circuit. (250, 301) are first circuit substrates, (251, 302) are second circuit substrates, and (303) is a third circuit substrate.

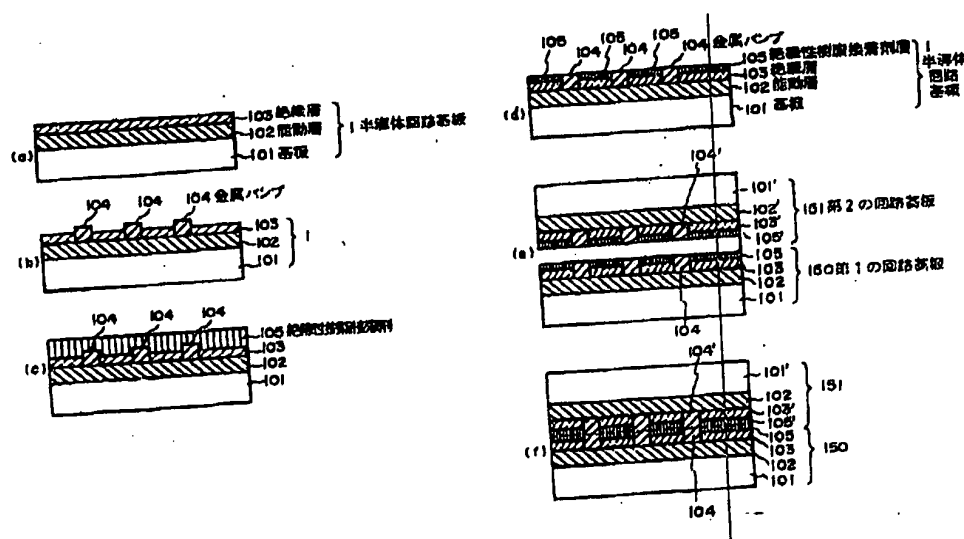


Figure 1

- Key:
- 1 Semiconductor circuit substrate
 - 101 Substrate
 - 102 Active layer
 - 103 Insulating layer
 - 104 Metallic bump
 - 105 Insulating resin adhesive layer
 - 150 First circuit substrate
 - 151 Second circuit substrate

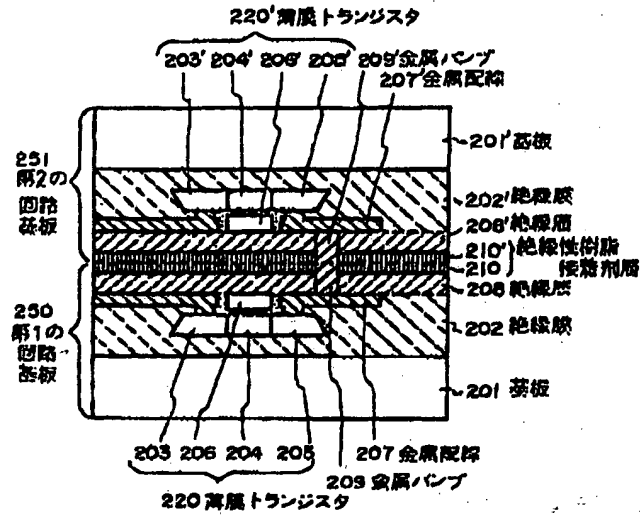


Figure 2

Key:	201, 201'	Substrate
	202, 202'	Insulating film
	207, 207'	Metallic wiring
	208, 208'	Insulating layer
	209, 209'	Metallic bump
	210, 210'	Insulating resin adhesive layer
	220, 220'	Thin film transistor
	250	First circuit substrate
	251	Second circuit substrate

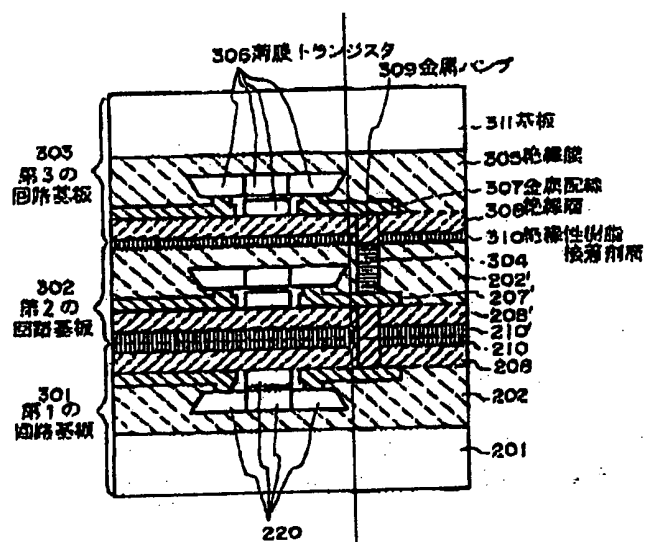
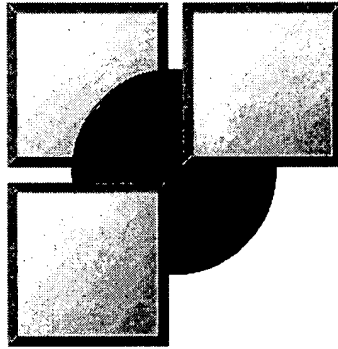


Figure 3

- Key:
- 301 First circuit substrate
 - 302 Second circuit substrate
 - 303 Third circuit substrate
 - 305 Insulating film
 - 306 Thin film transistor
 - 307 Metallic wiring
 - 308 Insulating layer
 - 309 Metallic bump
 - 310 Insulating resin adhesive layer
 - 311 Substrate



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